Features

- **Serial Peripheral Interface (SPI) Compatible**
- **Supports SPI Modes 0 (0,0) and 3 (1,1)**
  - **Data Sheet Describes Mode 0 Operation**
- **Low-voltage and Standard-voltage Operation**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **20 MHz Clock Rate (5V)**
- **8-byte Page Mode**
- **Block Write Protection**
  - **Protect 1/4, 1/2, or Entire Array**
- **Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: One Million Write Cycles**
  - **Data Retention: 100 Years**
- **Automotive Devices Available**
- **8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3) and 8-lead TSSOP Packages**
- **Die Sales: Wafer Form, Waffle Pack, Bumped Wafers**

Description

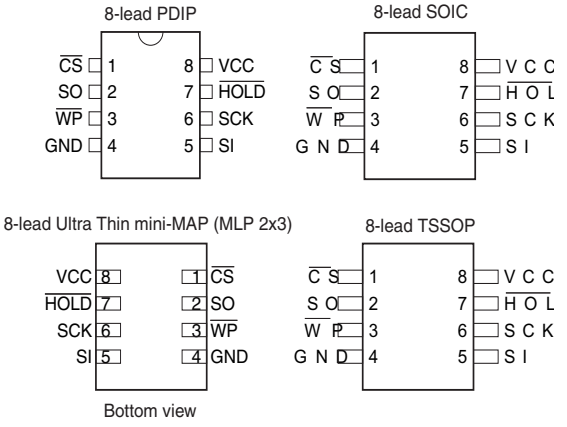
The AT25010A/020A/040A provides 1024/2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM) organized as 128/256/512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25010A/020A/040A is available in space saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), and 8-lead TSSOP packages.

The AT25010A/020A/040A is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate Program Enable and Program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Table 1. Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input



SPI Serial EEPROM

1K (128x8)

2K (256x8)

4K (512x8)

AT25010A
AT25020A
AT25040A

Absolute Maximum Ratings*

Operating Temperature	–40°C to + 125°C
Storage Temperature	–65°C to + 150°C
Voltage on Any Pin with Respect to Ground	–1.0V to + 7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram

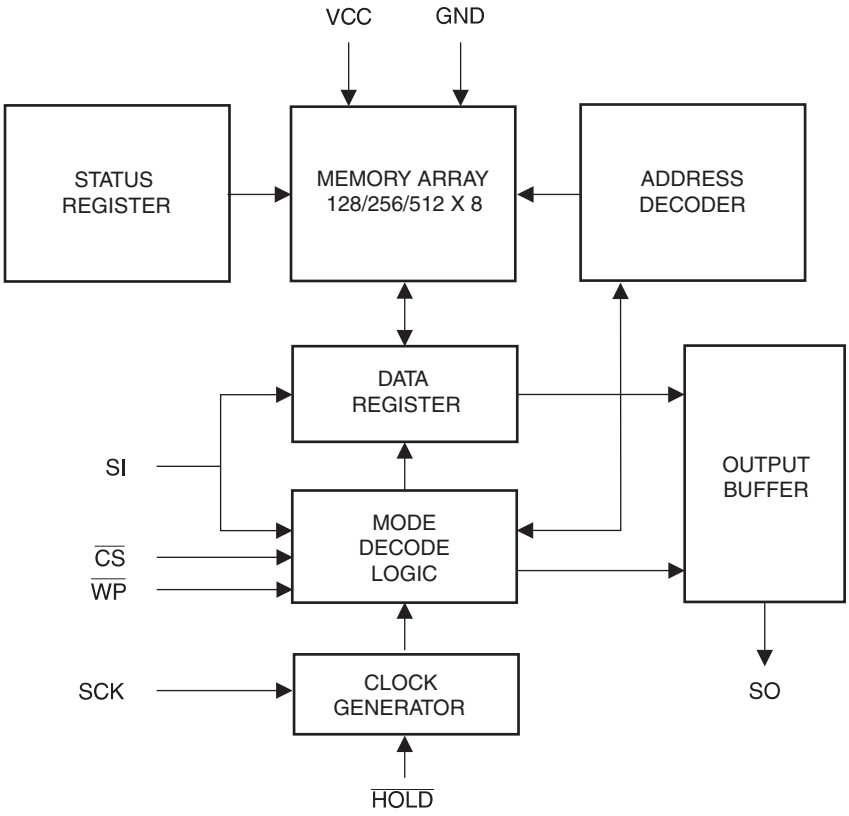


Table 2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics[1]

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 20 MHz, SO = Open, Read			8.5	10.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 10 MHz, SO = Open, Read, Write			4.5	5.0	mA
I_{CC3}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open, Read, Write			2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.1	0.5	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.2	1.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	3.5	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0			µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL}[1]	Input Low-voltage			–0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6 mA	V_{CC} – 0.8			V
V_{OL2}	Output Low-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics
Applicable over recommended operating range from T_{AI} = –40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	20 40 80		ns
t_{CS}	$\overline{CS}$ High Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	100 100 200		ns
t_{SU}	Data In Setup Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	20 40 80		ns
t_H	Data In Hold Time	4.5 – 5.5 2.7 - 5.5 1.8 - 5.5	20 40 80		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	20 40 80		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	20 40 80		ns
t_V	Output Valid	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	0 0 0		ns

Table 4. AC Characteristics (Continued)
Applicable over recommended operating range from T_{AI} = –40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5	0 0 0	25 50 100	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5		25 50 100	ns
t_{DIS}	Output Disable Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5		25 50 100	ns
t_{WC}	Write Cycle Time	4.5 – 5.5 2.7 – 5.5 1.8 – 5.5		5 5 5	ms
Endurance[1]	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

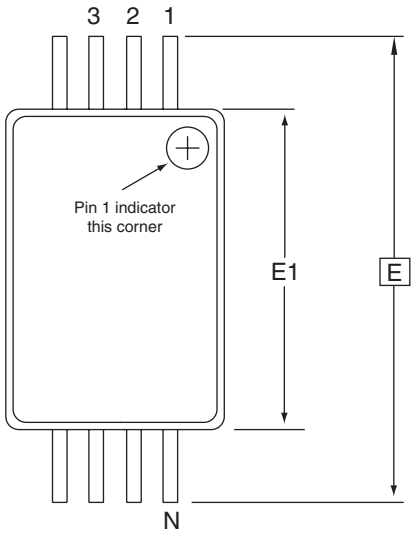
AT25010A Ordering Information[1]

Ordering Code	Package	Operation Range
AT25010A-10PU-2.7[2]	8P3	Lead-free/Halogen-free/ Industrial Temperature (−40 to 85°C)
AT25010A-10PU-1.8[2]	8P3	
AT25010AN-10SU-2.7[2]	8S1	
AT25010AN-10SU-1.8[2]	8S1	
AT25010A-10TU-2.7[2]	8A2	
AT25010A-10TU-1.8[2]	8A2	
AT25010AY1-10YU-1.8[2] (Not recommended for new designs)	8Y1	
AT25010AY6-10YH-1.8[3]	8Y6	
AT25010A-W1.8-11[4]	Die Sale	Industrial Temperature (−40 to 85°C)

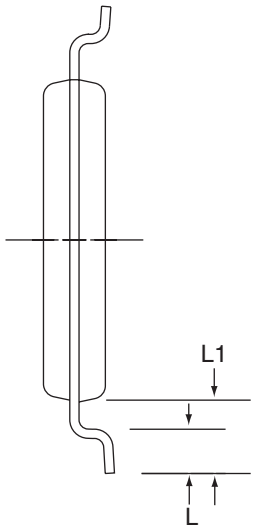
Notes:
1. For 2.7V devices used in the 4.5 to 5.5V range, please refer to performance values in Table on page 3 and Table 4 on page 4.
2. “U” designates Green Package + RoHS compliant.
3. “H” designates Green Package + RoHS compliant, with NiPdAu Lead Finish.
4. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial EEPROM Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8Y1	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm)
Options	
–2.7	Low Voltage (2.7 to 5.5V)
–1.8	Low Voltage (1.8 to 5.5V)

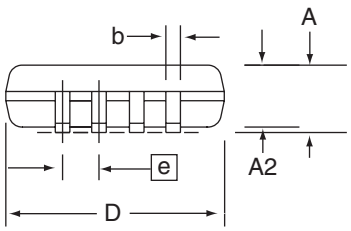
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B